REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-19 and 21-24 are pending in the application. The Examiner additionally stated that claims 1-19 and 21-24 are rejected. By this amendment, claims 1, 7, 11, 18, and 22 have been amended. Hence, claims 1-19 and 21-24 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

Non-Compliant Amendment

Applicant appreciates the Examiner's patience while the undersigned practitioner learned the new rules for amendment practice.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1-19 and 21-24 under 35 U.S.C. 103(a) as being unpatentable over Hammond et al., U.S. Patent Number 5,638,525 (hereinafter, "Hammond") in view of Patterson and Hennessy's Computer Architecture: A Quantitative Approach Second Edition, © 1996 (hereinafter, "Hennessy").

Applicant respectfully traverses the Examiner's rejections.

Referring to claim 1, the Examiner noted that Hammond has taught an apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor via an external instruction bus (Hammond column 4, lines 16-45 and Figure 1), the apparatus comprising:

> a. Instruction translation logic (Hammond column 17, lines 25-48 and 57-63; and Figure 7), configured to retrieve macro instructions provided via the external instruction bus (Hammond column 17, lines 25-48 and 57-63; and Figure 7), and

configured to decode each of said macro instructions into associated native instructions for execution by the microprocessor (Hammond column 17, lines 25-48 and 57-63; and Figure 7), wherein said instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions (Hammond column 4, line 61 to column 5, line 8; column 5, lines 54-60; column 6, lines 41-49; column 8, lines 54-60; column 18, lines 7- 18; and Figure 2), and

b. Bypass logic (Hammond column 17, lines 25-48 and 57-63; and Figure 7), coupled to said instruction translation logic (Hammond column 17, lines 25-48 and 57-63; and Figure 7), configured to disable said instruction translation logic upon detection of said native bypass macro instruction (Hammond column 17, lines 25-48 and 57-63; and Figure 7), and configured to provide the programmed native instructions for execution by the microprocessor, thereby bypassing said instruction translation logic (Hammond column 17, lines 25-48 and 57-63; and Figure 7).

The Examiner further wrote that Hammond has not taught wherein said memory address is explicitly prescribed by contents of an architectural register, said contents and said architectural register being prescribed by a macro instruction, but that Hennessy has taught wherein said memory address is explicitly prescribed by contents of an architectural register (Hennessy page 82, paragraph 2), said contents and said architectural register being prescribed by a macro instruction (Hennessy page 82, paragraph 2). The Examiner opined that person of ordinary skill in the art at the time the invention was made, and as taught by Hennessy, would have recognized that indirect jumps allow branch, jump, and other similar types of control flow instructions to still operate correctly even when the compiler does not know the exact address to jump to at the time of compile (Hennessy page 82, paragraph 2). The Examiner concluded that a person of ordinary skill in the art at the time the invention was made would have incorporated the indirect jumps of Hennessy in the device of Hammond in order to be

able to jump to the correct address even when the address is not known at the time the program is compiled.

Claim 1, as amended herein, is repeated below for ease of reference:

1. An apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor via an external instruction bus, the apparatus comprising:

instruction translation logic, configured to retrieve macro instructions provided via the external instruction bus, and configured to decode each of said macro instructions into associated native instructions for execution by the microprocessor, wherein said instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions, and wherein said memory address is explicitly prescribed by contents of an architectural register, said contents and said architectural register being prescribed by a macro instruction; and

bypass logic, coupled to said instruction translation logic, configured to disable said instruction translation logic upon detection of said native bypass macro instruction, and configured to provide the programmed native instructions directly to execution logic for execution, thereby bypassing said instruction translation logic.

Applicant respectfully disagrees with the Examiner's characterization of the teachings of Hammond and offers the following points in traversal of the rejection of claim 1. First, Hammond's invention is directed towards a processor that has the capability of accepting an application program with instructions from multiple instruction sets (col. 1, lines 50-52). More specifically, Hammond teaches his invention in the context of the two instruction sets being either a complex instruction set architecture (CISC) or reduced instruction set architecture (RISC) and he uses x86 move from and move to instructions to teach how operands are moved from one architectural resource to the next when

operation is switched between the two instruction set architectures (see Table I). In all of the teachings of Hammond, it is clearly evident that instructions fetched from memory are either translated or decoded into some form of "micro" or "native" instructions that are subsequently provided to an execution unit for execution (see Figures 3-7 and corresponding description of translator and/or decoder referenced thereby). Thus, Hammond fails to contemplate, consider, or even suggest that it is possible to provide native instructions directly from memory to execution logic in a microprocessor, where the native instructions are executed by the execution logic. This is because Hammond disclosures different instruction sets, all of which require either translation or decoding into some form of instruction that can be provided directly to execution logic.

In contrast to the teachings of Hammond, the invention of claim 1 recites, in combination with other elements and limitations, bypass logic that disables instruction translation logic upon detection of a native bypass macro instruction, and that provides programmed native instructions directly to execution logic for execution, thereby bypassing the instruction translation logic. Hammond does not teach any technique for completely bypassing instruction translation logic and providing programmed native instructions directly to execution logic for execution.

With regard to the teachings of Hennessey, Applicant concedes that the author teaches indirect jumps to allow branch, jump, and other similar types of control flow instructions to still operate correctly even when a compiler does not know the exact address to jump to at the time of compile. But Applicant also notes that Hennessey does not suggest, allude to, or even hint that such a technique can be employed in a microprocessor to enable a complete bypass of translation logic thereby enabling native instructions to be provided directly to execution logic for execution.

Thus, Hammond fails to teach a essential limitations of the invention of claim 1 and Hennessey provides no motivation whatsoever that would lead one skilled in the art to employ indirect techniques in a microprocessor having the capability to provide native instructions directly from memory to execution logic for execution. For these reasons, Applicant respectfully requests that the Examiner withdraw the rejection of claim 1.

With respect to claims 2-10, these claims depend from claim 1 and add further limitations that are neither anticipated nor made obvious by Hammond, Hennessey, or Hammond and Hennessey in combination. Accordingly, Applicant respectfully requests that the rejections of claims 2-10 be withdrawn.

Independent claims 11 and 18 are also amended herein to specifically recite that native instructions fetched from memory are provided directly to execution logic for execution according to the present invention, thus bypassing translation logic. In that the teachings of Hammond and Hennessey, alone and in combination, fail to teach this aspect of the present invention, Applicant respectfully requests that the rejections of claims 11 and 18 be withdrawn as well.

With respect to claims 12-17, these claims depend from claim 11 and add further limitations that are neither anticipated nor made obvious by Hammond, Hennessey, or Hammond and Hennessey in combination. Accordingly, Applicant respectfully requests that the rejections of claims 12-17 be withdrawn.

Likewise, claims 19 and 21-24 depend from claim 18 and add further limitations that are neither anticipated nor made obvious by Hammond, Hennessey, or Hammond and Hennessey in combination. Accordingly, Applicant respectfully requests that the rejections of claims 19 and 21-24 be withdrawn.

CONCLUSIONS

In view of the arguments advanced above, Applicant respectfully submits that claims 1-19 and 21-24 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
HUFFMAN PATENT GROUP, LLC

/Richard K. Huffman/

By: _____

RICHARD K. HUFFMAN, P.E.
Registration No. 41,082
Tel: (719) 575-9998

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Date: _____